

## REMARKS

Receipt of the Office Action of September 20, 2005 is gratefully acknowledge.

New claims 3 and 4 have been examined. These have been rejected as follows: (1) claims 3 and 4 as indefinite under 35 U.S.C. § 112 because a number of terms have no antecedent basis; and (2) claims 3 and 4 as unpatentable under 35 U.S.C. § 103(a) by Alsup in view of Meyer.

(1)

Claims 3 and 4 have been carefully amended to address the various objections raised by the examiner in enumerated paragraph 2 of the Office Action. In addition, claim 4 has been amended to remove the confusion created by the recitation of "cycle/cycles before the last cycle" in line 10 and "in the last cycle" in line 16. These deletions should clarify the scope of claim 4.

As amended, claims 3 and 4 are believed to be in full compliance with the provisions of 35 USC 112.

(2)

The noted rejection is respectfully traversed.


The Alsup patent does teach a method for performing register renaming with back-up capability. But Alsup does not teach a pipelining of register renaming process. In col. 6, line 44 to col., 7, line 65 their is described remapping of logical destination registers to physical registers and writing the results of the remapping into map cells. Then in col. 8, lines 3 - 67 a "back-up" operation is described, which is performed when an exception condition or branch prediction error occurs. This disclosure, however, does not match what is disclosed and claimed in the present application. Referring to page 6 of the specification, beginning on line 11 to page 9, line 3, it is noted that actual tags

@1, @2, @3 and @4 correspond to F registers F1, F2, F3 and F4, the orders of four instructions that are to go through the process of register renaming simultaneously. These tags are used only in the course of a pipelined register renaming process. A "tag" in the context of the present invention could be identified with an "offset tag" disclosed in Meyer et al (col. 7, lines 14 - 19), but not with the source register tag mentioned in col. 15, line 62 to col. 16, line 6 of Meyers et al. As to col. 16, lines 50 - 65 of Meyer et al, it is not clear why this passage is relevant at all in light of Alsup et al. Consider that the present invention breaks the register renaming process into multiple stages and pipelines these stages. By pipelining it is possible to process a large number of instructions per clock cycle. Where is step (b), at the very least, found in Alsup et al or Meyer et al? It is respectfully submitted that it is not found in either reference, so that it is certainly not found in their combination.

The examiner is urged, in view of the foregoing, to reconsider his art rejection and find that claims 3 and 4 comply with the provisions of 35 USC 112, and patentably distinguish over the combination of Alsup et al and Meyer et al. Alternatively, the examiner is urged to enter the above amendments to claims 3 and 4 for purpose of appeal.

Date: December 15, 2005

Respectfully submitted,  
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